CLAIMS: I claim:

1. A machine used for digital-to-analog conversion, comprising:
   a. a first counter which provides a first count
   b. a first analog reference source which provides a first analog reference signal
   c. a first digital number value to be converted to a first analog value
   d. means for causing said first count to change as a function of time
   e. means for causing said first analog reference signal to change as a function of time
   f. means for detecting when said first count reaches said first digital number value
   g. means for recording the value of said first analog reference signal as said first analog value when said first count reaches said first digital number value

   whereby said first analog value is the converted value of said first digital number value.

2. The machine of claim **1** in which said first analog reference source comprises a first current source charging a first capacitor, whereby said means for causing said first analog reference signal to change as a function of time is said first current source and whereby said first analog reference signal is a voltage across said first capacitor.

3. The machine of claim **1** wherein said means for causing said first count to change as a function of time is a first digital clock.

Sub B27

4. The machine of claim **3** in which said first digital clock has a frequency that can vary, whereby the machine of claim **1** can be used for digital-to-analog conversion of varying precision without the need for said first counter to always change at the fastest possible rate.

5. The machine of claim **1** in which said first analog reference source comprises a voltage ramp.

6. The machine of claim **1** in which said first analog reference source comprises an operational amplifier.

7. The machine of claim **1** in which said first analog reference source comprises a first digital-to-analog converter, whereby said first count can be the input to said first digital-to-analog converter and whereby said first analog reference signal can be the output of said first digital-to-analog converter.

8. The machine of claim **1** wherein said means for detecting when said first count reaches said first digital number value is a first logic circuit:
   a. said first logic circuit providing a first logic circuit output value when said first count is not equal to said first digital number value
   b. said first logic circuit providing a second logic circuit output value when said first count is equal to said first digital number value
   c. said first logic circuit output value not being the same as said second logic circuit output value

   whereby simple logical operations such as layered XNOR and AND operations can be used to make a digital comparator as said means for detecting when said first count reaches said first digital number value in said first logic circuit.

9. The machine of claim **1** wherein said means for recording the value of said first analog reference signal as said first analog value is a first sample-and-hold circuit.

10. The machine of claim **1** in which said first count controls said first analog reference source, whereby said first count need not be in increasing order or in decreasing order.

11. The machine of claim **1** in which said first count does not control said first analog reference signal, whereby said first count should be in increasing order or in decreasing order with said first analog reference signal level changing correspondingly.

12. The machine of claim **1** further including:

a. a second digital number value to be converted to a second analog value

b. means for detecting when said first count reaches said second digital number value

c. means for recording the value of said first analog reference signal as said second analog value when said first count reaches said second digital number value

whereby said first analog value and said second analog value are recorded from said first analog reference signal when said first count corresponds to said first digital number value and said second digital number value respectively, whereby parallel digital-to-analog conversion is implemented with said first counter and said first analog reference signal both being shared.

13. The machine of claim **12** in which:

a. said means for recording the value of said first analog reference signal as said first analog value when said first count reaches said first digital number value is a first sample-and-hold circuit

b. said means for recording the value of said first analog reference signal as said second analog value when said first count reaches said second digital number value is a second sample-and-hold circuit

whereby separate sample-and-hold circuits are used to record said first analog value and said second analog value.

14. The machine of claim **12** wherein:

a. said means for detecting when said first count reaches said first digital number value is a first logic circuit:

i. said first logic circuit providing a first logic circuit output value when said first count is not equal to said first digital number value

ii. said first logic circuit providing a second logic circuit output value when said first count is equal to said first digital number value

iii. said first logic circuit output value not being the same as said second logic circuit output value

b. said means for detecting when said first count reaches said second digital number value is a second logic circuit:

i. said second logic circuit providing a third logic circuit output value when said first count is not equal to said second digital number value

ii. said second logic circuit providing a fourth logic circuit output value when said first count is equal to said second digital number value

iii. said third logic circuit output value not being the same as said fourth logic circuit output value

whereby simple logical operations such as layered XNOR and AND operations can be used to make a digital comparator as said means for detecting when said first count reaches said first digital number value in said first logic circuit and as said means for detecting when said first count reaches said second digital number value in said second logic circuit.

15. The machine of claim **14** in which:

a. said first logic circuit output value is the same value as said third logic circuit output value

b. said second logic circuit output value is the same value as said fourth logic circuit output value

whereby said first logic circuit and said second logic circuit can have identical structures, allowing a standard design for logic circuits used as digital comparators.

16. The machine of claim **12** in which said second digital number value has a different number of representation elements than said first digital number value, whereby digital-to-analog conversion of said first digital number value to said first analog value and digital-to-analog conversion of said second digital number value to said second analog value can have differing precision, but can still share circuitry such as said first counter.

17. The machine of claim **1** further including:

a. a second analog reference source which provides a second analog reference signal
b. a second digital number value to be converted to a second analog value
c. means for causing said second analog reference signal to change as a function of time
d. means for detecting when said first count reaches said second digital number value
e. means for recording the value of said second analog reference signal as said second analog value when said first count reaches said second digital number value

whereby said first analog value and said second analog value are recorded from said first analog reference signal and from said second analog reference signal when said first count corresponds to said first digital number value and when said first count corresponds to said second digital number value respectively, whereby parallel digital-to-analog conversion is implemented with said first counter being shared.

18. The machine of claim **17** in which said first analog reference signal and said second analog reference signal have different values, whereby digital-to-

analog conversion of said first digital number to said first analog value and digital-to-analog conversion of said second digital number to said second analog value have differing conversion mappings from digital numbers to analog values.

19. The machine of claim **1**, further including means for causing said first digital number value to change as a function of time, whereby said first analog value is the converted value of said first digital number value prior to its change with time, and represents the time required for the difference between the time-varying first count and the time-varying first digital number value to reach zero.

20. A machine used for digital-to-analog conversion, comprising:

a. a first counter which provides a first count
b. means for initializing said first count to a first digital number value
c. a first analog reference source which provides a first analog reference signal
d. means for causing said first count to change as a function of time
e. means for causing said first analog reference signal to change as a function of time
f. means for detecting when said first count reaches a first digital threshold value
g. means for recording the value of said first analog reference signal as said first analog value when said first count reaches said first digital threshold value

whereby said first analog value is the converted value of said first digital number value.

21. The machine of claim **20** further including:

a. a second counter which provides a second count
b. means for initializing said second count to a second digital number value

c. means for causing said second count to change as a function of time
d. means for detecting when said second count reaches a second digital threshold value
e. means for recording the value of said first analog reference signal as said second analog value when said second count reaches said second digital threshold value

whereby said first analog value is the converted value of said first digital number value and whereby said second analog value is the converted value of said second digital number value.

22. The machine of claim **21** in which said first digital threshold value is the same as said second digital threshold value.

23. The machine of claim **22** in which said first digital threshold value is equal to zero.

24. The machine of claim **20** further including:

a. a second counter which provides a second count
b. a second analog reference source which provides a second analog reference signal
c. means for initializing said second count to a second digital number value
d. means for causing said second count to change as a function of time
e. means for causing said second analog reference signal to change as a function of time
f. means for detecting when said second count reaches a second digital threshold value
g. means for recording the value of said second analog reference signal as said second analog value when said second count reaches said second digital threshold value

whereby said first analog value is the converted value of said first digital number value and whereby said second analog value is the converted value of said second digital number value.

25. The machine of claim **24** in which said first digital threshold value is the same as said second digital threshold value.

26. The machine of claim **25** in which said first digital threshold value is equal to zero.

27. A digital-to-analog converter comprising a first circuit element, wherein:

a. said first circuit element is used in a first instance for a first conversion of a first digital number to a first analog value

b. said first circuit element is also used in said first instance for a second conversion of a second digital number to a second analog value

c. said first circuit element comprises a first parameter that varies with time during a conversion operation

whereby said first circuit element is effectively shared in said first conversion and in said second conversion, rather than used in said first instance for said first conversion and separately in a second instance for said second conversion, and whereby said first circuit element is not simply a constant reference signal.

28. The digital-to-analog converter of claim **27** in which said first circuit element is a first counter.

29. The digital-to-analog converter of claim **28**, further including:

a. a first digital comparator providing a first digital comparator output

b. means for averaging said first digital comparator output over time

whereby said digital-to-analog converter can implement shared parallel pulse-width modulation digital-to-analog conversion.

30. An analog-to-digital converter comprising the digital-to-analog converter of claim **27**, whereby parallel analog-to-digital conversion of a multiplicity of analog values to a multiplicity of digital number values can share said first circuit element, such as parallel successive-approximation or half-flash analog-to-digital converters.

31. The digital-to-analog converter of claim **27** in which said first circuit element is a first analog reference source.

32. A machine used for digital-to-analog conversion, comprising:

a. a first counter which provides a first count
b. means for initializing said first count to a first digital number value
c. means for causing said first count to change as a function of time
d. means for detecting when said first count reaches a first digital threshold value
e. means for averaging the output of said means for detecting when said first count reaches a first digital threshold

whereby the output of said means for averaging is the converted value of said first digital number value.

33. The machine of claim **32** in which said means for detecting when said first count reaches a first digital threshold value is a first digital comparator.

34. The machine of claim **32** in which said first digital threshold level is zero, whereby no storage means are necessary to hold the value of said first digital threshold level and whereby said means for detecting when said first count reaches said first digital threshold level can be implemented with simple digital logic such as a single multiple-input AND gate.